**Amendments to the Claims:**

This listing of claims will replace all prior version, and listings, of claims in the application. Where claims have been amended and/or canceled, such amendments and/or cancellations are done without prejudice and/or waiver and/or disclaimer to the claimed and/or disclosed subject matter, and the applicant and/or assignee reserves the right to claim this subject matter and/or other disclosed subject matter in a continuing application.

**Listing of Claims:**

1. (Previously amended): An integrated circuit package comprising:

(a) an integrated circuit die having at least one circuit etched thereon, the circuit comprising elements which require theoretically negative reactive component values; and

(b) a housing containing said integrated circuit die, wherein said integrated circuit die is electrically coupled to said housing using at least one wire bond; and wherein each wire bond has an inductance associated therewith; and wherein the negative reactive component values theoretically required by the integrated circuit are actually incorporated into the circuit through the use of wire bonds having pre-determined inductance values.

2. (Previously amended): The integrated circuit of claim 1, wherein the circuit comprises an impedance inverter.

Claims 3-13 (Canceled)

14. (New): An apparatus, comprising:

a first inductor disposed in a series arrangement;

a second inductor coupled to said first inductor at a first node of said first inductor, said second inductor being disposed in a shunt arrangement; and

a third inductor coupled to said first inductor at a second node of said first inductor, said third inductor being disposed in a shunt arrangement;

wherein said first inductor comprises at least one or more wire bonds coupled to an integrated circuit of an integrated circuit package.

15. (New): An apparatus as claimed in claim 14, at least one of said second inductor or said third inductor, or combinations thereof, being disposed on the integrated circuit.

16. (New): An apparatus as claimed in claim 14, at least one of said second inductor or said third inductor, or combinations thereof, being disposed external to the integrated circuit.

17. (New): An apparatus as claimed in claim 14, at least one of said second inductor or said third inductor, or combinations thereof, being disposed on the integrated circuit and another one of said second inductor or said third inductor, or combinations thereof, being disposed external to the integrated circuit.

18. (New): An apparatus as claimed in claim 14, both of said second inductor and said third inductor being disposed on the integrated circuit.

19. (New): An apparatus as claimed in claim 14, both of said second inductor and said third inductor being disposed external to the integrated circuit.

20. (New): An apparatus as claimed in claim 14, at least one or more of said second inductor or said third inductor, or combinations thereof, comprising a negative valued inductance.

21. (New): An apparatus as claimed in claim 14, at least one or more of said second inductor or said third inductor, or combinations thereof, comprising a shunt capacitance to realize a negative valued inductance.

22. (New): An apparatus as claimed in claim 14, at least one of said second inductor or said third inductor, or combinations thereof, comprising a spiral inductor.

23. (New): An apparatus as claimed in claim 14, said first inductor, said second inductor, and said third inductor comprising an impedance inverter capable of transforming a lower output impedance to a higher output impedance.

24. (New): An apparatus as claimed in claim 14, one or more of said wire bonds being configured to provide a predetermined impedance value.

25. (New): An apparatus as claimed in claim 14, one or more of said wire bonds comprising a configuration capable of providing a predetermined impedance value, the

configuration comprising one or more of shape, length, or thickness, or combinations thereof.

26. (New): An apparatus, comprising:

a semiconductor wafer;

an integrated circuit formed on said semiconductor wafer;

a package at least partially containing said semiconductor wafer;

a first inductor disposed in a series arrangement;

a second inductor coupled to said first inductor at a first node of said first inductor, said second inductor being disposed in a shunt arrangement; and

a third inductor coupled to said first inductor at a second node of said first inductor, said third inductor being disposed in a shunt arrangement;

wherein said first inductor comprises at least one or more wire bonds coupled to said integrated circuit and at least partially disposed within said package.

27. (New): An apparatus as claimed in claim 26, at least one of said second inductor or said third inductor, or combinations thereof, being disposed on said integrated circuit.

28. (New): An apparatus as claimed in claim 26, at least one of said second inductor or said third inductor, or combinations thereof, being disposed external to said integrated circuit.

29. (New): An apparatus as claimed in claim 26, at least one of said second inductor or said third inductor, or combinations thereof, being disposed on the integrated circuit and another one of said second inductor or said third inductor, or combinations thereof, being disposed external to said integrated circuit.

30. (New): An apparatus as claimed in claim 26, both of said second inductor and said third inductor being disposed on said integrated circuit.

31. (New): An apparatus as claimed in claim 26, both of said second inductor and said third inductor being disposed external to said integrated circuit.

32. (New): An apparatus as claimed in claim 26, at least one or more of said second inductor or said third inductor, or combinations thereof, comprising a negative valued inductance.

33. (New): An apparatus as claimed in claim 26, at least one or more of said second inductor or said third inductor, or combinations thereof, comprising a shunt capacitance to realize a negative valued inductance.

34. (New): An apparatus as claimed in claim 26, at least one of said second inductor or said third inductor, or combinations thereof, comprising a spiral inductor.

35. (New): An apparatus as claimed in claim 26, said first inductor, said second inductor, and said third inductor comprising an impedance inverter capable of transforming a lower output impedance to a higher output impedance.

36. (New): An apparatus as claimed in claim 26, one or more of said wire bonds being configured to provide a predetermined impedance value.

37. (New): An apparatus as claimed in claim 26, one or more of said wire bonds comprising a configuration capable of providing a predetermined impedance value, the configuration comprising one or more of shape, length, or thickness, or combinations thereof.

38. (New): An apparatus as claimed in claim 26, further comprising a carrier pad, said first inductor being coupled to said carrier pad.

39. (New): An apparatus as claimed in claim 26, further comprising a carrier pad, at least one of said second inductor or said third inductor, or combinations thereof, being disposed on said carrier pad.

40. (New): An apparatus as claimed in claim 26, further comprising a carrier pad, at least one of said second inductor or said third inductor, or combinations thereof, being disposed on said carrier pad, and another one of said second inductor or said third inductor being disposed on said integrated circuit.

41. (New): An apparatus as claimed in claim 26, said package comprising one or more of a quad flat pack, a ball grid array, or a flip chip, or combinations thereof.